CLAIM CHANGES:

1. (Previously Cancelled)

2. (Previously Cancelled)

3. (Previously Cancelled)

4. (Previously Cancelled)

5. (Previously Cancelled)

C'

6. (Previously Cancelled)

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10. (Previously Cancelled)

11. (Previously Cancelled)

12. (Previously Cancelled)

13. (Previously Cancelled)

14. (Previously Cancelled)

15. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

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forming an etching mask constituted by a first insulating film having an opening portion including a gate forming portion and source/drain extension regions forming portion on a surface of a semiconductor substrate;

forming a trench in ~~said~~ the semiconductor substrate in correspondence with the opening portion of ~~said~~ the etching mask;

forming a gate insulating film constituted by a second insulating film on an inner surface of ~~said~~ the trench;

forming a gate material film on ~~said~~ the second insulating film;

patterning ~~said~~ the gate material film to form a gate on a central portion between both sides of ~~said~~ the trench on a source/drain side through ~~said~~ the second insulating film;

implanting impurity ions into at least a bottom surface of ~~said~~ the trench by using ~~said~~ the gate as a mask to form source/drain extension regions;

forming a third insulating film to cover ~~a~~ the surface of ~~said~~ the semiconductor substrate ~~subjected to the steps~~;

forming gate sidewall spacers constituted by ~~said~~ the third insulating film by using anisotropic etching to cover the inner surface of the trench extending on the source/drain side of ~~said~~ the gate; and

implanting impurity ions into the source/drain regions by using ~~said~~ the gate having the gate sidewall spacers as a mask to form a MIS-type field effect transistor having source/drain regions being close to or adjacent to side surfaces of the trench of ~~said~~ the semiconductor substrate and connected to the source/ drain extension regions on the bottom surface of ~~said~~ the trench in which a position where an impurity concentration of the source/drain regions in the direction of depth is maximum almost coincides with a position where an impurity concentration of the source/drain extension regions in the direction of depth is maximum .

16. (Currently Amended) A method of manufacturing a semiconductor device according to claim 15, wherein ~~said~~ the trench is formed by isotropic etching such that the side surfaces of ~~said~~ the trench on the source/drain side constitute a rounded surface.

17. (Currently Amended) A method of manufacturing a semiconductor device according to claim 15, wherein ion implantation for threshold voltage control of ~~said~~ the MIS-type field effect transistor is performed to only the bottom surface of ~~said~~ the trench.

18. (Currently Amended) A method of manufacturing a semiconductor device according to claim 15, wherein ~~said~~ the first, second, and third insulating films are an SiO_2

film formed by an LPCVD method using TEAS, an SiO_2 film formed by thermal oxidation of silicon, and an SiN film formed by a CVD method, respectively.

19. (Currently Amended) A method of manufacturing a semiconductor device according to claim 15, wherein ~~said~~ the first insulating film is formed to be stacked on a thermal oxidation film formed as a buffer layer on ~~said~~ the semiconductor substrate.

20. (Currently Amended) A method of manufacturing a semiconductor device according to claim 15, further comprising ~~the steps of,~~ after a silicide film of high melting point metal is formed on a silicon surface exposed to the source/drain regions and upper surfaces of ~~said~~ the gate consisting of polysilicon by forming a high melting point metal film to cover the surface of ~~said~~ the semiconductor substrate and performing heat treatment, removing ~~said~~ the high melting point metal film remaining on the gate sidewall spacers.

21. (Previously Cancelled)

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31. (Previously Cancelled)

32. (Previously Cancelled)

33. (Previously Cancelled)

34. (Previously Cancelled)

35. (Newly Added) A method of manufacturing a semiconductor device according to claim 15, wherein an allowable misfit range required to make the maximum positions coincide with each other is about $\pm$ 0.01 μm with respect to the conditions for perfect coincidence.